Parallel Dynamic Logic(PDL) with Speed-Enhanced Skewed Static (SSS) Logic*

Chulwoo Kim, Seong-Ook Jung, Kwang-Hyun Baek, and Sung-Mo(Steve) Kang
University of Illinois at Urbana-Champaign
Department of Electrical and Computer Engineering, Coordinated Science Laboratory
1308 W, Main St., Urbana, IL 61801

Abstract

In this paper, we describe Parallel Dynamic Logic (PDL) which exhibits high speed, no charge sharing problem. PDL uses only parallel-connected transistors for logic evaluation and is a good candidate for high-speed low-voltage operation. It has less back-bias effect compared to other logic styles which use stacked transistors. Furthermore, PDL needs no signal ordering nor tapering. PDL with speed-enhanced skewed static logic renders straightforward logic synthesis without area penalty due to logic duplication. Our experimental results on two 32-bit carry lookahead adders using 0.25μm CMOS technology showed that PDL with speed-enhanced skewed static (SSS) logic improves performance over clock-delayed(CD)-domino by 15-27% and power×delay by 20-37%.

1 Introduction

Conventional static CMOS circuits are slow because each gate must drive both NMOS and PMOS transistors. Domino logic circuits, however, drives only NMOS transistors, so it has the advantage of faster operation and smaller area compared to conventional CMOS circuits. Domino logic circuits have been widely used for high-performance microprocessors and other logic chips. However, it has drawbacks which include an inherently non-inverting nature, strict timing constraints, and charge sharing. Several dynamic logic circuits have been proposed and their potential for practical applications has been cited in [1] – [4]. NORA circuits generate inverting logic only by strictly cascading NMOS and PMOS dynamic gates [2]. Although dual-rail logic circuits provide inverting and non-inverting outputs, the area cost of a gate is about twice that of a standard domino gate, since both the inverting and non-inverting outputs are generated [4]. Furthermore, power consumption of dual-rail logic is another bottleneck for practical use. Clock-delayed(CD) domino eliminates the fundamental monotonic signal requirement by propagating a clock network in parallel to the logic [3]. Although CD domino circuits provide both inverting and non-inverting signals, it is very difficult to design the clock-delayed scheme because the clock delay should be large enough to allow evaluation of the slowest of the gates. Furthermore, clock-delayed scheme is very sensitive to process and needs additional circuits. We propose a parallel dynamic logic and speed-enhanced skewed static gates which use positive feedback to enhance the speed of skewed static gates.

This paper is organized as follows. Section II describes the conventional dynamic gates and cascading problem of them.

*This research was supported in part by a grant from Semiconductor Research Corp. under SRC contract No. 98-HJ-641

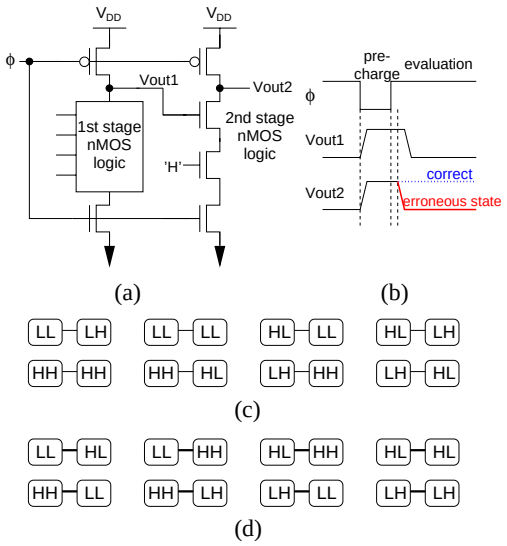


Figure 1: Illustrations of the cascading problem in dynamic CMOS logic (a) schematic of cascaded circuits (b) timing diagram (c) combinations of cascadable dynamic gates (d) combinations of uncascadable dynamic gates, thick line means uncascadable connection

In section III and IV, we explain PDL and SSS circuit concept and show the simulation results of them. In section V, two 32-b CLAs using conventional CD-domino and proposed circuits have been designed and their simulation results are presented. Finally, conclusions are drawn in section VI.

2 Conventional Dynamic Circuits

As shown in Fig. 1, all dynamic gates cannot be cascaded directly because each dynamic gate is precharged to a high logic level which causes a discharge of output of next stage dynamic gates [6]. If the evaluation transistors of a dynamic gate consist of only NMOS, all inputs for that gate should be a low logic level, 'L', and if PMOS, a high logic level, 'H'. Let us define several types of dynamic gates as 'XY' gate. 'X' is related to logic level of inputs to the gate during precharge phase and 'Y' is related to logic level of outputs of the gate during precharge phase. If the output is precharged to low logic level, then 'Y' is 'L', and, if high, 'H'. We can cascade each gate only if $Y_{(i)} = X_{(j)}$, where $i < j$, which means the output of previous gates should have the same type of input of the gate as shown in Fig. 1(c) and (d).

To solve cascading problem of dynamic gate, Krambeck et al. proposed domino which includes static inverter followed by each dynamic gate as shown in Fig. 2. Although domino has no cascading problem, one of the limitations of this circuit technique is that all of the gates are non-inverting

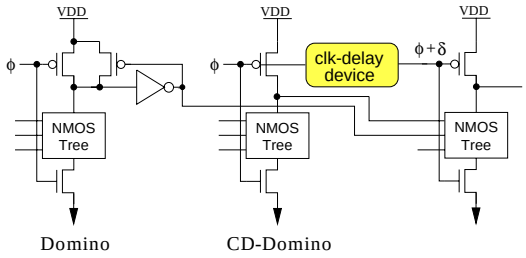


Figure 2: Conventional cascading problem solutions

[1]. NORA provides non-inverting gates, but the number of static inversions between the last dynamic block in a logic function and the C^2MOS latch should be even.

From our definition of 'XY' gate, domino logic has 'LL' AND gate and 'LL' OR gate. In conventional domino, because all gates are 'LL' type, we can cascade any gates but we have only non-inverting gates. NORA has both 'LH' gates which uses NMOS transistors for evaluation and 'HL' gates which uses PMOS transistors for evaluation, but has to be used by strictly cascading NMOS and PMOS NORA gates.

In CD domino, we have 'LH' NOR gate, 'LH' NAND gate, 'LL' OR gate, and 'LL' AND gate. 'LH' NOR gate, however, cannot be cascaded with 'LH' NOR gate nor 'LH' NAND gate without delayed-clock as we explained in Fig. 1(d). In CD domino, this problem is solved by inserting a delay between clocks as shown in Fig. 2. Each CD domino gate consists of a dynamic gate and a clock-delay logic device if necessary. The CD domino gate can be either non-inverting(domino type) or inverting without an inverter at the output. The delay is set equal to the worst case pull-down delay of the corresponding dynamic gate, plus a margin for variations in fabrication processes, differences in the signal delay due to wire routing, and coupling parasitics. Hence, clock-delay scheme prevents further speed enhancement and it is not easy to set an amount of clock-delay per stage.

3 Parallel Dynamic Logic

To get high-performance under low-voltage operation, we propose parallel dynamic logic (PDL). The basic PDL gates are illustrated in Fig. 3. Two clock signals with 180° phase difference are used in PDL as in NORA. There are, however, several differences between PDL and NORA. In NORA, NMOS block is followed by PMOS block and vice versa. And there are stacked transistors in PMOS NOR/OR gate and NMOS NAND/AND gate in NORA. Each PDL gate adopts parallel type topology which improves performance because of non-stack scheme for logic evaluation. Due to parallel topology, PDL has no charge sharing problem which is common in other dynamic logic circuits. To overcome the threshold voltage drop and to obtain a full logic level at the output node, static inverter and transistors Mp and Mn are used in OR gate and AND gate, respectively. For further speed improvement, positive feedback circuits can be used as an inverter.

In general, the multiple-input parallel-connected transistors can be reduced to one equivalent transistor for static analysis. The (W/L) ratio of the equivalent transistor is

$$\left(\frac{W}{L}\right)_{parallel,equi} = \sum_{k(on)} \left(\frac{W}{L}\right)_k \quad (1)$$

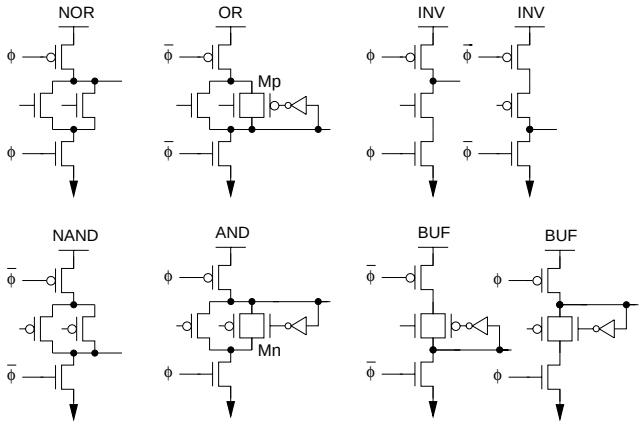


Figure 3: PDL gates

For multiple-input serially connected transistors, neglecting the substrate-bias effect and assuming that the threshold voltages of all transistors are equal to V_{T0}, the (W/L) ratio of the equivalent transistor is

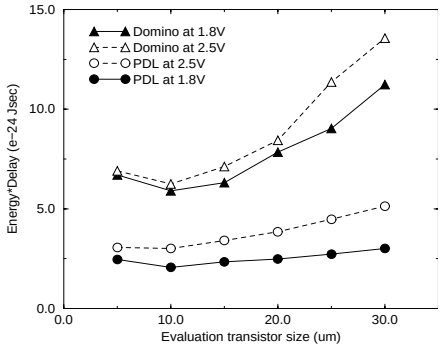
$$\left(\frac{W}{L}\right)_{stacked,equi} = \frac{1}{\sum_{k(on)} \frac{1}{\left(\frac{W}{L}\right)_k}} \quad (2)$$

From above equations, for an n-input stacked topology, each transistor must have a (W/L) ratio n-times that of the equivalent transistor. The resulting n-input stacked topology will occupy approximately n-times the area occupied by the n-input parallel topology. Furthermore, this increases the input gate capacitance n-times and interconnect capacitance as well which cause speed degradation and higher power consumption. Although NAND gates using stacked NMOS transistors in NORA, domino, and CD-domino or NOR gates using stacked PMOS transistors in NORA consist of n times larger evaluation transistors, all of the PDL gates consist of basic size transistors for evaluation. V_T of stacked transistors varies a lot due to back bias effect which degrades the circuit performance as well. Therefore, PDL gates show higher speed compared to domino, NORA, and CD-domino.

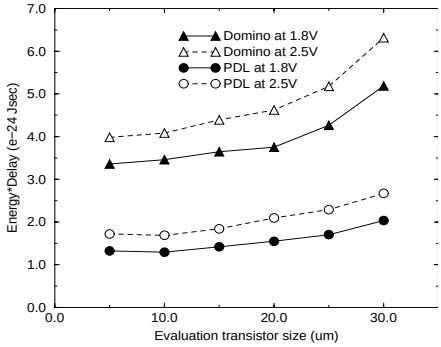
In real chip implementation, input signals usually arrive at different time. For stacked topology, output evaluation cannot be done until the final input signal comes to the gate of one of the stacked transistors. But for PDL, if any of input signal arrives at the gate of parallel connected transistors, output starts to be evaluated and the evaluation can be even finished before the latest input signal arrives if the difference of input signal arriving time is bigger than gate delay. This is an additional advantage when we cascade PDL in complex systems. In sub-1V technology, leakage current becomes a serious problem due to low V_T of transistors. Although PDL adopts a parallel structure, leakage problem is not significant because PDL still can use high V_T transistors under sub-1V operation. Simulation results for PDL with 4-input OR/AND gates with all inputs tied are shown in Fig. 4. It shows that PDL OR/AND gates have 1.8 $\sim$ 3.7 times less energy×delay than domino and CD-domino gates depending on transistor sizes and supply voltages. Usage of PDL gates for wide gates such as 64-bit zero/one detectors can provide drastic speed enhancement.

4 Speed-enhanced Skewed Static Logic

As shown in Fig. 3, in PDL, AND gate is 'HH' type, OR gate is 'LL' type, NAND gate is 'HL' type and NOR gate



(a)



(b)

Figure 4: Simulation results of 4-input gates (a) OR gate (b) AND gate

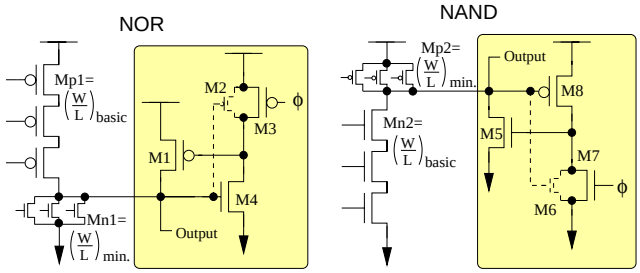


Figure 5: SSS Logic gates

is 'LH' type. Although PDL has better performance compared to conventional dynamic logic, it has cascading problem as well. Clock-delay can be adopted in PDL, but there are several disadvantages as we explained before. Therefore, we propose speed-enhanced skewed static logic circuits which give more flexibility to solve the cascading problem. The SSS circuit examples are illustrated in Fig. 5. SSS circuits are composed of two main parts, the logic function and positive feedback for speed enhancement which is the shaded area in Fig. 5. The logic circuit is the same as the skewed CMOS static circuit whose trip point is deviated from (Vdd/2) for fast transition and therefore sizes of transistor Mn1s' and Mp2s' are smaller than normal CMOS circuit. Because the output node is driven by positive feedback circuit, sizes of Mp1 and Mn2 do not need to be increased as shown in (2). Therefore, SSS gate has less input capacitance than that of domino. Positive feedback circuits, which are shaded in Fig. 5, consist of feedback transistors (M1, M4/ M5, M8) and one precharge transistor (M3/ M7). Small transistors M2 and M6 ensure stable operation by preventing the floating of the output nodes. Output node of SSS

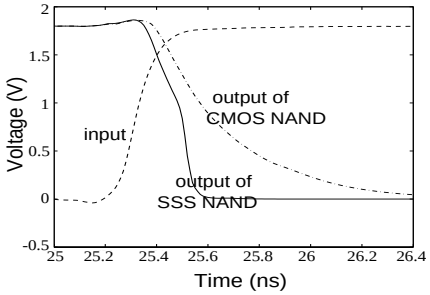


Figure 6: Simulation results of 8-input NAND gates

circuit is precharged by input signals during precharge phase of dynamic circuit and transits only in one direction during the evaluation phase of dynamic circuit. SSS circuits, hence, provide better performance compared to CMOS static circuits. Even SSS circuit may have a cascading problem when its fanout is connected to 2 opposite precharged state at the same time. Fig. 6 shows that SSS 8-input NAND gate is 36% faster than CMOS one.

5 Comparisons of 32-bit Adders using CD-domino and PDL with SSS circuit

Adder is an essential basic building block in digital systems. Therefore, we have designed and simulated 32-bit carry-lookahead adders using 0.25μm CMOS technology to show the efficiency of our proposed circuit technique in actual applications. Fig. 7(a) shows the block diagram of a 32-bit CLA using CD-domino and PDL with SSS circuit. In CD-domino adder, with the availability of high fan-in NOR gates, ADD4×8 can be improved with the faster NOR gates, as indicated in (3) [3]. Therefore, the longest path of a 32-b adder is reduced to 8 simple gates from 12 simple gates which is the case of normal domino gates(maximum number of input is 4). In the equations, +, $\otimes$, and $\oplus$ represents OR, XNOR and XOR, respectively.

$$
\begin{aligned}
&\overline{g_i} = \overline{a_i} + \overline{b_i}, \quad \overline{p_i} = \overline{a_i} \otimes \overline{b_i}, \quad s_i = \overline{p_i} \oplus \overline{c_i}, \quad \overline{c_0} = \overline{c_{in}},\\
&\overline{c_1} = \overline{g_0 + (\overline{p_0} + \overline{c_{in}})}, ...,\\
&\overline{c_7} = \overline{g_6 + (\overline{p_6} + \overline{g_5}) + ... + (\overline{p_6} + ... + \overline{p_0} + \overline{c_{in}})}\\
&\overline{P_0} = \overline{p_7} + \overline{p_6} + \overline{p_5} + \overline{p_4} + \overline{p_3} + \overline{p_2} + \overline{p_1} + \overline{p_0}, ...,\\
&\overline{P_3} = \overline{p_{31}} + \overline{p_{30}} + \overline{p_{29}} + \overline{p_{28}} + \overline{p_{27}} + \overline{p_{26}} + \overline{p_{25}} + \overline{p_{24}}\\
&\overline{G_0} = \overline{g_7 + (\overline{p_7} + \overline{g_6}) + ... + (\overline{p_7} + \overline{p_6} + ... + \overline{p_1} + \overline{g_0})}, ...,\\
&\overline{G_3} = \overline{g_{31} + (\overline{p_{31}} + \overline{g_{30}}) + ... + (\overline{p_{31}} + \overline{p_{30}} + ... + \overline{p_{25}} + \overline{g_{24}})}\\
&\overline{C_1} = \overline{G_0 + (\overline{P_0} + \overline{c_{in}})}, ...,\\
&\overline{C_4} = \overline{G_3 + (\overline{P_3} + \overline{G_2}) + ... + (\overline{P_3} + ... + \overline{P_0} + \overline{c_{in}})} \qquad (3)
\end{aligned}
$$

As shown in above equations, all of inputs to a 32-bit CLA using CD-domino must be inverted and this causes additional inversion delay if there is no inverted input signal. Fig. 7 shows of 32-b CLAs using CD-domino, PDL, and PDL with SSS circuit. Thick line means each stage cannot be cascaded directly as shown in Fig. 1(d). In Fig. 7(b), although node $\overline{G1}$ is precharged to 'H', node G1 is precharged 'L', so the inverter can be cascaded to 'LH' NOR gate without any problem. As shown in Fig. 7(b),(e), different amount of clock-delays are needed for every stage in the 32-b CLA using CD-domino. In a 32-b CLA using PDL, with the availability of high fan-in AND/NAND gates, (3) can be modified as follows. In the equations, · represents AND.

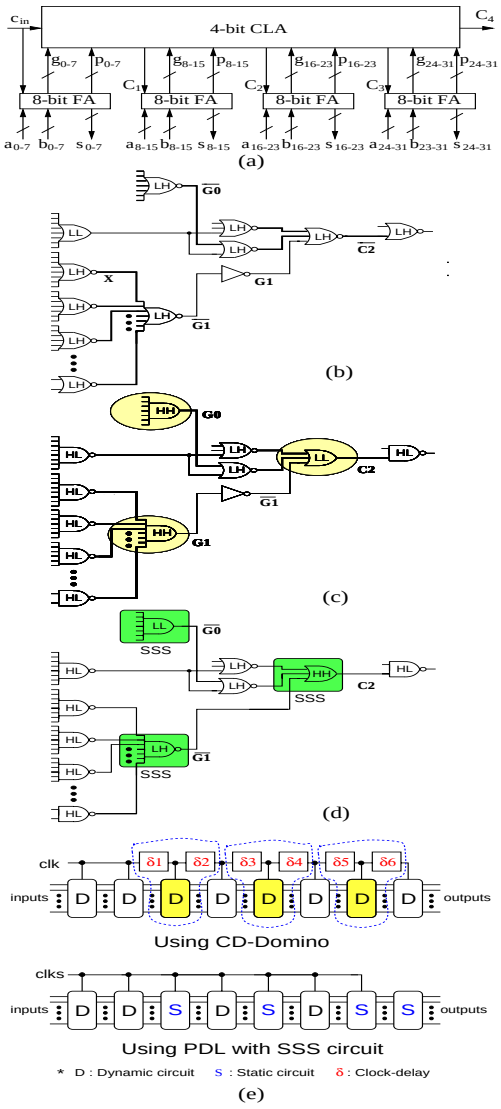


Figure 7: Schematic of 32-b CLAs (a) block diagram (b) using CD-domino (c) using PDL (d) using PDL with SSS circuit (e) comparison of clock schemes for the entire path

$$
\begin{aligned}
g_i &= a_i \cdot b_i, \quad p_i = a_i \oplus b_i, \quad s_i = p_i \oplus c_i, \quad c_0 = c_{in}, \\
c_1 &= g_0 \cdot \overline{(p_0 \cdot c_{in})}, \ldots, \; c_7 = g_6 \cdot \overline{(p_6 \cdot g_5)} \cdot \ldots \cdot \overline{(p_6 \cdot \ldots \cdot p_0 \cdot c_{in})} \\
\overline{P_0} &= \overline{p_7} \cdot \overline{p_6} \cdot \overline{p_5} \cdot \overline{p_4} \cdot \overline{p_3} \cdot \overline{p_2} \cdot \overline{p_1} \cdot \overline{p_0}, \ldots, \\
\overline{P_3} &= \overline{p_{31}} \cdot \overline{p_{30}} \cdot \overline{p_{29}} \cdot \overline{p_{28}} \cdot \overline{p_{27}} \cdot \overline{p_{26}} \cdot \overline{p_{25}} \cdot \overline{p_{24}} \\
G_0 &= \overline{\overline{g_7} \cdot \overline{(p_7 \cdot g_6)} \cdot \ldots \cdot \overline{(p_7 \cdot p_6 \cdot \ldots \cdot p_1 \cdot g_0)}}, \ldots, \\
G_3 &= \overline{g_{31} \cdot \overline{(p_{31} \cdot g_{30})} \cdot \ldots \cdot \overline{(p_{31} \cdot p_{30} \cdot \ldots \cdot p_{25} \cdot g_{24})}} \\
C_1 &= G_0 + \overline{(\overline{P_0} + \overline{c_{in}})}, \ldots, \\
C_4 &= \overline{G_3 + \overline{(\overline{P_3} + \overline{G_2})} + \ldots + \overline{(\overline{P_3} + \ldots + \overline{P_0} + \overline{c_{in}})}}
\end{aligned}
\tag{4}
$$

Part of 32-b CLA using PDL is shown in Fig. 7(c). In this case, we have similar cascading problem as in Fig. 7(b). SSS circuits can be used to replace PDL gates in the shaded area as shown in Fig. 7(c) and (d). As a result, proposed scheme removes all of 6 clock-delays by replacing one dynamic gate and two clock-delays with one SSS gate as shown in Fig. 7(e). Both adders using CD-Domino and PDL with SSS circuit occupy almost equal die area, and we have estimated the parasitic capacitances and interconnect capacitances for

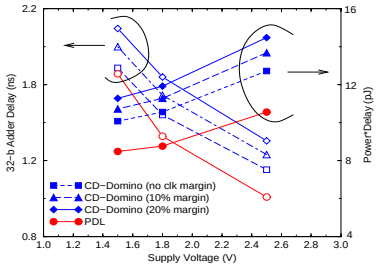


Figure 8: Simulation results of 32-b CLAs

HSPICE simulations. For both the adders, the width of evaluation transistors were 10μm. As illustrated in Fig. 8, the 32-bit adder using the proposed circuit technique consumes 20% to 37% less energy than the CD-domino adder over various power supply voltages. In real implementation, however, 20% clock-delay margin is required for proper operation [3]. In that case, our proposed technique consumes 37% less energy as shown in Fig. 8.

6 Conclusions

We have proposed PDL which exhibits high speed and no charge sharing problem due to the use of only-parallel-connected transistors. SSS circuits were also proposed and they give more flexibilities for cascading dynamic circuits. We designed two 32-bit CLAs using 0.25μm CMOS technology to verify the area and performance efficiency of PDL with SSS circuits in real applications. Simulation results showed that an adder using the proposed circuit design consumes 20% to 37% less energy than CD-domino adder at various power supply voltages. Design automation for the proposed circuit architecture can be achieved easily because of their flexibility for cascading and complete logic families. PDL with SSS circuits are good candidates for high-speed low-voltage digital logic in sub-1V technology.

Acknowledgments

We express our gratitude to Seung-Moon Yoo in UIUC for his constructive comments.

References

[1] R. H. Krambeck, C. M. Lee, and H-F. S. Law, "High-Speed Compact Circuits with CMOS," in *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 614-619, Jun. 1982.

[2] N. F. Goncalves and H. J. De Mari, "NORA: A Racefree Dynamic CMOS Technique for Pipelined Logic Structure," in *IEEE J. Solid-State Circuits*, vol. 18, pp. 261-266, Jun. 1983.

[3] Gin Yee and Carl Sechen, "Clock-Delayed Domino for Adder and Combinational Logic Design," in *IEEE International Conference on Computer Design 1996*, pp. 332-337.

[4] L. G. Heller, W. R. Griffin, J. W. Davis, and N. G. Thoma, "Cascode Voltage Switch Logic : A Differential CMOS Logic Family," in *IEEE J. Solid-State Circuits*, vol. 19, pp. 16-17, Jun. 1984.

[5] R. Puri, A. Bjorksten, and T. E. Rosser, "Logic Optimization by Output Phase Assignment in Dynamic Logic Synthesis," in *IEEE/ACM International Workshop Logic Synthesis*, pp. 2-8, May 1997.

[6] Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, 2nd ed., McGraw-Hill, 1999.